PMICRO
Powerlink Microelectronics

PL51RC103

ADC/Touch Key
Low Power High Performance
13.56MHz Contactless
Reader SOC

Product Description:

PL51RC103 is a highly integrated contactless (13.56MHz) reader SOC. This transmission module utilizes the principles of modulation and demodulation，and fully integrate into variety of contactless communication methods and protocols(13.56MHz). Transmission module support reader mode and ISO14443A/MIFARE®.

PL51RC103 combines 13.56MHz reader module, a single-cycle enhanced 8051 compliant CPU, 16KB in-system programmable flash memory, 256B EEPROM data memory, 256B IRAM, 1KB XRAM, up to 18 General-Purpose I/O pins, the program and data area read control permission can be configured, and the program area code encryption scrambling storage, high security level to protect user program and data.

PL51RC103 internal transmitter part drives the reader antenna communication with ISO14443A/MIFARE® card and transponder without additional circuit. Receiver part provided a powerful and efficient demodulation and decoding circuit for processing signals from ISO14443A/MIFARE® card and transponder. Digital circuit part handles complete ISO14443A frame and error detection (parity & CRC).

PL51RC103 support MIFARE® Classic devices (MIFARE® standard).

PL51RC103 support MIFARE® high speed contactless communication with two-way data transfer rate up to 424kbit/s.

Built in power management function, the current consumption in power off and standby mode can be reduced to nearly 3uA.

Built in Crystal Oscillator resistor (680K), capacitances (2*15pF).

For easy usage, POWERLINK provides the debugger and writer.

PL51RC103 support UART, I2C and SPI interfaces.

PL51RC103 reader module support SPI/UART* interfaces communication.

Key Features:

- Contactless 13.56MHz Reader SOC
- Support ISO14443A/MIFARE®
- 1T Enhanced 8-bit ET8051
- 16KB Flash and 256B EEPROM
- Reader mode support MIFARE® Classic encryption
- Support ISO14443 212/424kbit/s
- 64B transmit and receiver FIFO buffer area
- Flexible interrupt mode
- Low-power hardware reset
- Software power-off mode
- CRC coprocessor
- Reader support UART/SPI
- Fully integrated up to 13 touch keys
- RF Operation Freq.@Voltage: ~27.12MHz@3.3V
- Operation Temperature: -25℃ ~+85℃
- Up to 18 bidirectional GPIO
- Three 16-bit Timers/Counters
- Six 12-bit PWM: PWM0/1/2/3/4/5
- Support UART/SPI/I2C interface
- Integrated 11-bit 9channels ADC
- Support ICP function
- Support ICD function
- Package: QFN6X6-36L
- Flash Cycling: 100K@25℃
- EEPROM Cycling: 500K@25℃
- Data retention: 40 years@25℃

Applications:

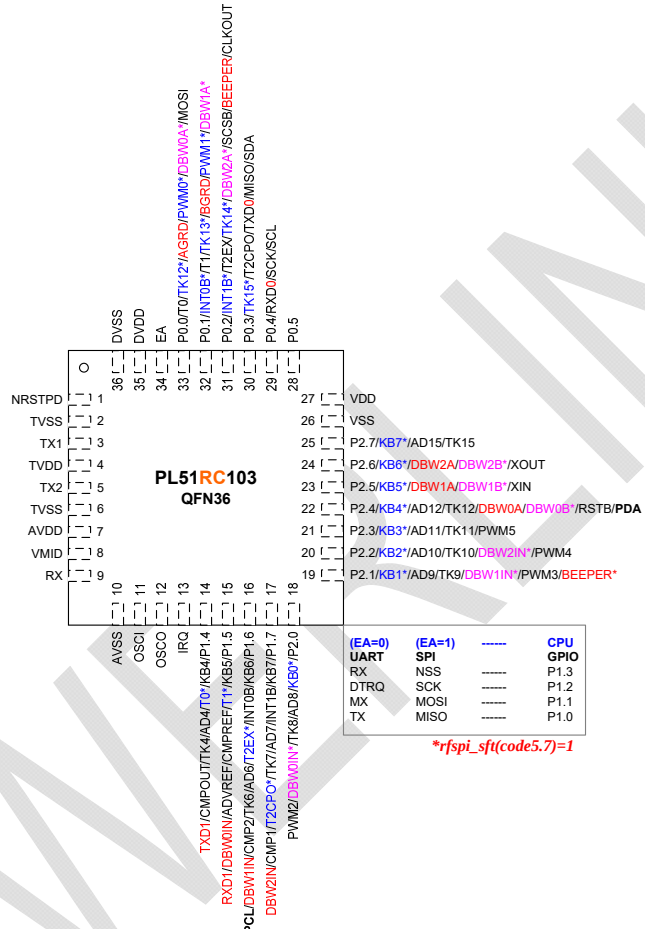
- Contactless 13.56MHz Reader

RoHS GREEN

Contents

1 Pin Configurations

1.1 Pin Diagrams



Note：

1) *The outside pin function has the highest priority, and the inner pin function has the lowest priority. It means that if the higher priority function is enabled, the lower priority function can't be used even when the lower priority function is also enabled.*

2) *The pin name colored blue with * denoted the shift ports, the pin function available only when the relative shift control bit in SFR "PSFT0~1" is set.*

3) *In the corner is the description of connection between MCU (PL51T103) and reader (PRC522) module pin.*

4) *Specially：this chip register AUXCON.s003_sopt cannot be set to 1.*

5) *For unused or not led out pins, recommended to configure input pull-up or output fixed lever.*

1.2 MCU (PL51T103) Pin Description

Symbol	Type	Descriptions
VCC	Power	Power Supply (2.4~3.6V)
VSS	Power	Ground (0V)
RSTB	Digital Input	Reset Input, active Low
XIN	Analog Input	Crystal Oscillator Input
XOUT	Analog Output	Crystal Oscillator Output
CLKOUT	Digital Output	Internal Clock Output
SCL	Digital I/O	Clock for I2C Interface
SDA	Digital I/O	Data I/O for I2C Interface
SCSB	Digital Input	Enable Input for SPI Interface, active Low
SCK	Digital I/O	Clock for SPI Interface
MISO	Digital I/O	Master Data Input or Slave Data Output for SPI Interface
MOSI	Digital I/O	Master Data Output or Slave Data Input for SPI Interface
RXD0/1	Digital Input	RXD0/1 of Serial Port
TXD0/1	Digital Output	TXD0/1 of Serial Port
T0	Digital Input	Timer 0 Input
T1	Digital Input	Timer 1 Input
T2 EX	Digital Input	Timer 2 external reload or gate Input
T2CPO	Digital Output	T2 compare or PWM output
INT0B	Digital Input	External Interrupt 0
INT1B	Digital Input	External Interrupt 1
PWM0~5	Digital Output	PWM 0~5 Output
DBW0A	Digital Output	Death Wave Generation DBW0A Output
DBW1A	Digital Output	Death Wave Generation DBW1A Output
DBW2A	Digital Output	Death Wave Generation DBW2A Output
DBW0B	Digital Output	Death Wave Generation DBW0B Output
DBW1B	Digital Output	Death Wave Generation DBW1B Output
DBW2B	Digital Output	Death Wave Generation DBW2B Output
DBW0IN	Digital Input	Death Wave Generation DBW0 Iutput
DBW1IN	Digital Input	Death Wave Generation DBW1 Iutput

Symbol	Type	Descriptions
DBW2IN	Digital Input	Death Wave Generation DBW2 Iutput
CMP1	Analog Input	Comparator channel 1 Input
CMP2	Analog Input	Comparator channel 2 Input
CMPVREF	Analog Input	Comparator Reference Input
CMPOUT	Digital Output	Comparator Output
TK0~15	Analog Input	13 channels Touch Key Inputs（Deleted TK5/TK13/TK14）
KB0~7	Analog Input	8 channels Keyboard Inputs
ADVREF	Analog Input	ADC Reference Voltage Input
AD0~15	Analog Input	9 channels ADC Analog Inputs（Deleted AD5/AD13/AD14）
BEEPER	Digital Output	BEEPER Output
P0.0~P0.5	Digital I/O	General purpose I/O Port 0
P1.0~P1.7	Digital I/O	General purpose I/O Port 1
P2.0~P2.7	Digital I/O	General purpose I/O Port 2
PCL	Digital Input	Clock Input for ICP/ICD Mode
PDA	Digital I/O	Data I/O for ICP/ICD Mode

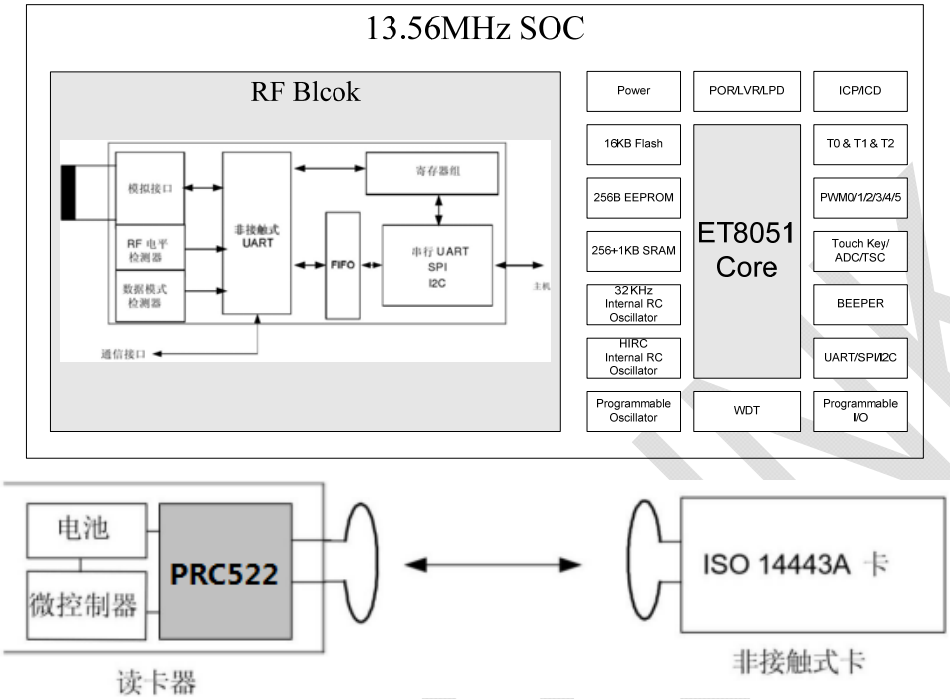
1.3 Reader module (PRC522) Pin Description

Symbol	HVQFN32	Type	Descriptions
OSCIN	21	I	Crystal Oscillator Input: Input of oscillator inverting amplifier. External clock input (f_{osc} = 27.12MHz)
IRQ	23	O	Interrupt Request: output, indicated an interrupt event
SIGIN	7	I	Signal Input
SIGOUT	8	O	Signal Output
TX1	11	O	Transmitter 1: transmit modulated 13.56MHz energy carrier signal
TVDD	12	PWR	Transmitter Power: supply power to TX1 and TX2 output
TX2	13	O	Transmitter 2: transmit modulated 13.56MHz energy carrier signal
TVSS	10,14	PWR	Transmitter Ground: ground of TX1 and TX2 output
DVSS	4	PWR	Digital Ground
D1	25	I/O	Data Pin for Different Interfaces (TEST port, I2C, SPI, UART)
D2	26	I/O	

Symbol	HVQFN32	Type	Descriptions
D3	27	I/O	
D4	28	I/O	
D5	29	I/O	
D6	30	I/O	
D7	31	I/O	
SDA	24	I	Data Input for I2C Interface
EA	32	I	External Address: this pin is used to encode I2C address
I2C	1	I	I2C Enable
DVDD	3	PWR	Digital Power
AVDD	3	PWR	Analog Power
AUX1	19	O	Auxiliary Output: those pin are used for testing
AUX2	20	O	
AVSS	18	PWR	Analog Ground
RX	17	I	Receiver Input: receive RF signal pin
VMID	16	PWR	Internal Reference Voltage: the pin supply internal reference voltage
NRSTPD	6	I	No Reset and Power-off: when pin is low, cut off internal current absorption, close oscillator, turn off the connection between input pin and external circuit. The rising edge of pin start internal reset phase.
OSCOUT	22	O	Crystal Oscillator Output: output of oscillator inverting amplifier.
TESTPIN	9		Unconnected: Tri-stated pin
PVDD	2	PWR	Pin Power
PVSS	5	PWR	Pin Ground

Note: *Pin type: I – Intput; O – Output; PWR – Power*

2 Block Diagram



The PRC522 transmit module support the reader mode of ISO14443A/MIFARE with a variety of transmission rate and modulation methods, and is a common card reader for card communication following ISO14443A/MIFARE.

The PRC522 support various microcontroller interfaces type, such as SPI, I2C and serial UART.

The PL51RC103 support SPI, I2C and UART interfaces; the internal MCU&RF communication interfaces of PL51RC103 support SPI (configure rfspi_sft(code5.7) as 1, internal direct connection) and UART (use MCU GPIO simulation, not recommend).

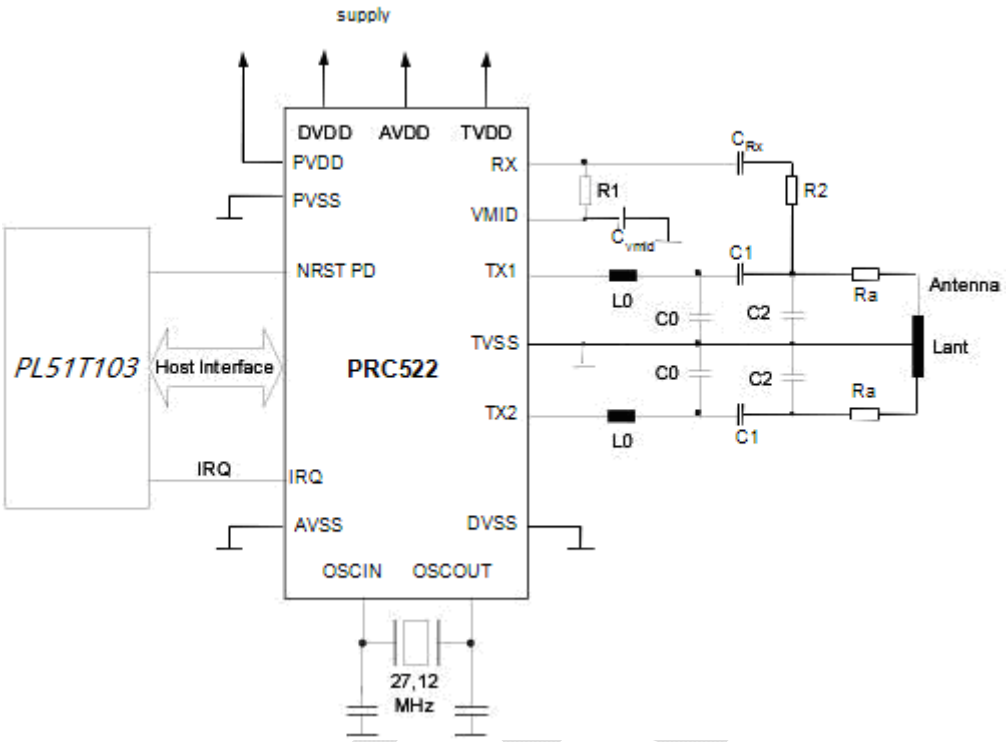
2.1 MCU Core Information

The detail description of MCU core is in PL51T103 user manual, please contact with POWERLINK.

2.2 RF Block Control Register Information

The latest recommended control registers value is in PRC522 user manual, please contact with POWERLINK.

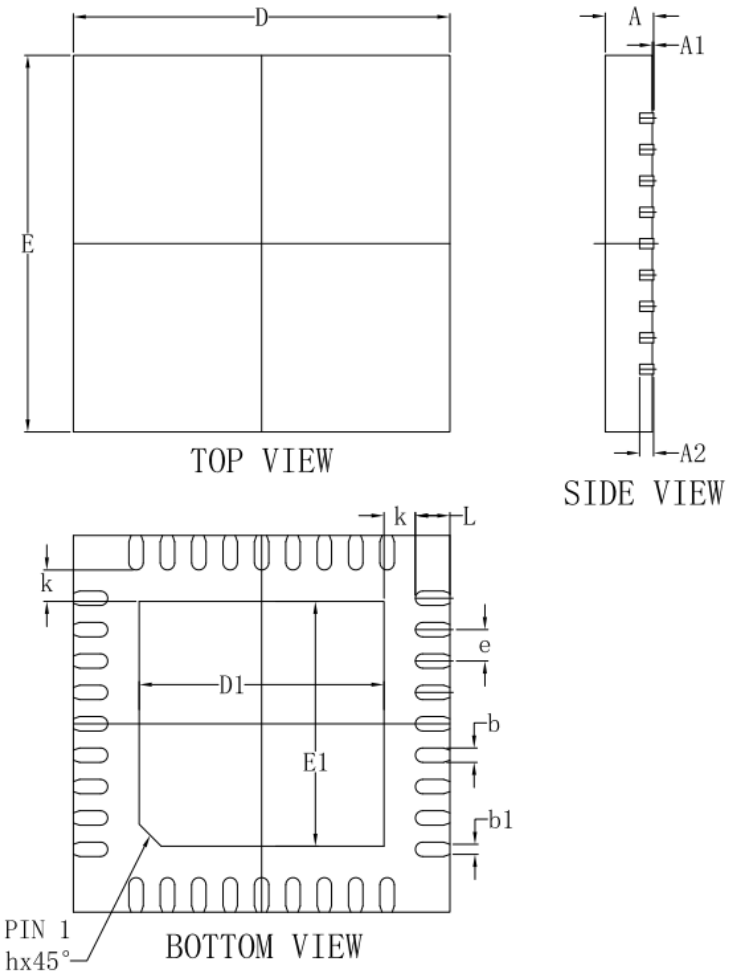
3 Typical Application



4 Package Dimensions

4.1 QFN6x6-36L Package

QFN6x6-36L PACKAGE OUTLINE DIMENSIONS



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	/	0.050
A2	0.173	0.203	0.253
b	0.180	0.230	0.280
b1	0.110	0.160	0.210
D	5.950	6.000	6.050
D1	3.850	3.900	3.950
E	5.950	6.000	6.050
E1	3.850	3.900	3.950
e	0.450	0.500	0.550
h	0.300	0.350	0.400
k	0.450	0.500	0.550
L	0.500	0.550	0.600

5 Ordering Information

Part Number	Packaging
PL51RC103N36	QFN6x6-36L, Tube
PL51RC103N36R	QFN6x6-36L, Tape&Reel

6 Document Revision History

Rev.	Date	Comments
0.1	2021/07/28	Initial Version
0.2	2021/09/29	Add Register AUXCON.s003_sopt Application Notice
0.3	2021/11/04	Updated Operation Parameter
0.4	2022/02/11	Updated Pin definition, Configure rfspi_sft Internal Direct Connection
0.5	2022/07/22	Deleted DAC/OPA's Pins
0.6	2023/02/06	Updated PL51T103's pin definition，Deleted TKADC-5&13&14

7 Important Notice

POWERLINK reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.