PMICRO
Powerlink Microelectronics

PL51WT103

ADC 型/电容触摸型
低功耗高性能 2.4GHz RF
无线射频收发 SOC

Product Description:

PL51WT103 is a ADC/Touch Key low power high performance 2.4GHz wireless system-on-chip (SOC) with operation in the world wide ISM frequency band at 2.400~2.4835GHz.

PL51WT103 combines 2.4GHz RF transceiver with a single-cycle enhanced 8051 compliant CPU, 16KB in-system programmable flash memory, 256B EEPROM data memory, 256B IRAM, 1KB XRAM, up to 15 General-Purpose I/O pins, program and data area read control permission, and program area code encryption scrambling storage, high security level to protect user program and data.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

Output power, channel selection and protocol can be flexible configured through SPI interface.

With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

Built in address and FEC, CRC function;

Built in Auto-ACK & Auto-Resend function.

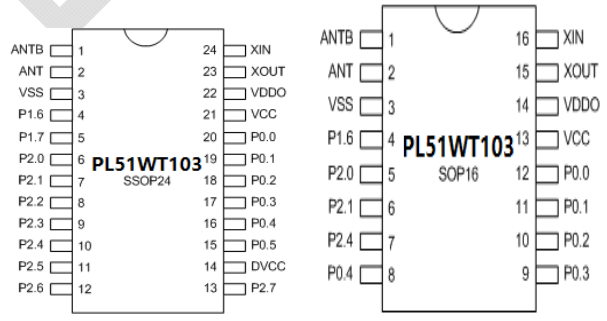
The output power of the chip can be set up to 5.5dBm and the receive sensitivity can achieve -88dBm.

Built in Crystal Oscillator resistor (680K), capacitances (2*15pF).

Built in 10K pull-down resistor for ANT and ANTB antenna.

PL51WT103 support UART, I2C and SPI interfaces.

Pin Configuration:



Key Features:

- 2.4GHz RF SOC with Touch Key
- 1T Enhanced 8-bit ET8051
- 16KB Flash and 256B EEPROM
- Data Rate over the Air：1Mbps
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-ACK and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Support HFSS
- 12MHz RF Crystal Oscillator
- Support Micro-Strip Inductor and Two Layer PCB Boards
- Fully integrated up to 8+4(shift) touch keys
- CPU Operation Freq.@Voltage: ~12MHz@2.7~3.6V
- Operation Temperature: -25℃ ~+105℃
- Up to 15 bidirectional GPIO
- Three 16-bit Timers/Counters
- Six 12-bit PWM: PWM0/1/2/3/4/5
- Support UART/SPI/I2C interface
- Integrated 11-bit 8 channels ADC
- Support ICP&ICD function
- Package: SOP16, TSSOP20, SSOP24
- Flash Cycling: 100K@25℃
- EEPROM Cycling: 500K@25℃
- Data retention: 40 years@25℃

Applications:

- Proprietary 2.4GHz Systems
- Wireless Mice, Keyboards and Game Controllers
- RF Remote Controller
- Home and Commercial Automation

RoHS GREEN

Product Types

Product Name	Package	Program Flash	Data EEPROM	RAM	Timer	PWM	Freq@Voltage	I/O	Interface UART/SPI/I2C	ACMP	T.S.	Touch Key*1 /Wakeup(Max)	ADC
PL51WT103B24	SSOP24	16KB	256B	256**B**+1K	3	6+1	~12M@2.4~3.6V	16	1/1/1	1	1	8+4*3/10	8
PL51WT103T20	TSSOP20	16KB	256B	256B+1K	3	6+1		13	1/1/1	1	1	6+4*3/5+4	6
PL51WT103S16	SOP16	16KB	256B	256B+1K	3	6+1		9	1/1/1	1	1	4+4*2/3+4	4

Note: **1: Touch Key can't work with ADC at the same time, but can be set to work separately at different time slice.*

**2: Shift Touch Keys <15:12> can be assigned as the touch keys <15:12> with wake-up function.*

**3: Shift touch keys <15:12> or Original ones can be set to work separately at different time slice. Only Shift touch keys <15:12> or Original ones can be assigned as wake-up keys, separately.*

**4: ACMP source, only between CMP1 and INTVREF (1.2V).*

Contents

1 Overview

PL51WT103 is a ADC/Touch Key low power high performance 2.4GHz wireless system-on-chip (SOC) with operation in the world wide ISM frequency band at 2.400~2.4835GHz.

PL51WT103 combines the excellent performance of a leading 2.4GHz RF transceiver with a single-cycle enhanced 8051 compliant CPU, 16KB in-system programmable flash memory, 256B EEPROM data memory, 256B IRAM, 1KB XRAM, up to 15 General-Purpose I/O pins and many other powerful features.

PL51WT103 fully integrated touch key functions eliminating the need for external components. Special algorithms are employed to reduce the possibility of false detections, increasing the touch switch application reliability under adverse environmental conditions. Support automatic calibration configuration, touch key can work in a wider dynamic capacitance range, while reducing power consumption and improving identification sensitivity. PL51WT103 provides a simple and effective means of implementing touch switches in a wide range of applications.

In-Circuit Programming ICP support user update program and data; the program and data area can be configured read control permission, and program area code encryption scrambling storage, high security level to protect user program and data.

This single chip wireless transceiver integrated including: RF synthesizer, Power Amplifier, Crystal Oscillator, Modem and etc.

All of the Output Power, Channel Selection, and Protocol of RF block can be configured through SPI Interface.

With built in FHSS and accurate digital RSSI, this transceiver achieves a good capability of anti-interference, so that, it can work under every complicated environment with high performance.

It also support address and data check out; FEC, CRC function; and Auto-ACK & Auto-Resend function.

The output power of the chip can be set up to 5.5dBm and the receive sensitivity can achieve -88dBm.

The 680K resistor and two 15pF capacitances are built in for 12MHz RF Crystal Oscillator.

The 10K pull-down resistor is built in for ANT and ANTB antenna.

PL51WT103 internal integrates high/low precision RC oscillator to operate and switch dynamically between a range of operating modes using different clock sources to optimize microcontroller operation and minimize power consumption.

PL51WT103 is communicating with the outside world with UART, I2C and SPI interfaces. The excellent noise immunity and ESD protection ensure reliable operations in the adverse electrical environments. Besides the flash program memory, other memory includes RAM Data Memory as well as EEPROM memory is integrated.

For high reliability and low cost issues, PL51WT103 builds in reliable watchdog timer (WDT) low power detect (LPD) and low voltage reset (LVR) function. To reduce power consumption, PL51WT103 also support three low power modes, idle, stop and sleep mode; support quick keyboard wakeup in low-power mode.

For easy usage, POWERLINK provides the debugger and writer.

PL51WT103 is targeting at the proprietary 2.4GHz systems such as Human Interface Devices, Wireless Mice, Keyboards and Game Controller, RF Remote Controller, Home and Commercial Automation and etc.

2 Features

RF

- True Low Power High Performance Single Chip 2.4GHz Transceiver
- Built in Hardware Link Layer
- Built in Accurate Digital RSSI
- Support Auto-ACK and Auto-Resend Functions
- Built in Address and Data Checkout, FEC, CRC Functions
- Data Rate over the Air：1Mbps
- Support HFSS
- Support Micro-Strip Inductor and Two Layer PCB Boards
- Built-in 680K resistor and two 15pF CAP for 12MHz RF Crystal Oscillator
- Built-in 10K pull-down resistor for ANT and ANTB antenna

Basic

- 1T 8-bit ET8051 compatible with MCS-51
- Fully integrated up to 8+4(shift) touch key functions with no external components
- CPU core Operation Frequency@Voltage: ~12MHz@2.4~3.6V
- Operation Frequency: ~12MHz
- Operation Temperature: -25℃ to +105℃
- CPU core Oscillator Type:
  - ✧ Crystal Oscillator: 400KHz to 12MHz
  - ✧ Internal RC Oscillator: 4/8/12MHz and 32KHz
  - ✧ External Clock: 400KHz~12MHz
- Up to 15 bidirectional General Purpose I/O
  - ✧ Input-Only with configurable pull high resistor
  - ✧ Push-Pull Output Drive Capacity: 10mA (@3V, Total: <100mA)

Peripheral Features

- Four Priority Levels with 16 interrupt sources
  - ✧ Two External Interrupt: INT0B and INT1B
  - ✧ T0&T1 Overflow Interrupt
  - ✧ T2 Overflow, Reload, Compare/Capture Interrupt
  - ✧ UART0&UART1 Transmit and Receive Interrupt
  - ✧ EEPROM Write Finished Interrupt
  - ✧ Analog Comparator Interrupt
  - ✧ Keyboard Interrupt
  - ✧ Touch Key Interrupt
  - ✧ SPI Interrupt
  - ✧ I2C Interrupt
  - ✧ ADC Finish Converting Interrupt
- POR/LVR/LPD support
- Eight LVR threshold Level by Fuse:

1.2/1.5/1.8/2.1/2.4/2.7/3.7/4.3V

- Eight LPD threshold Level by Fuse:

  1.2/1.5/1.8/2.1/2.4/2.7/3.7/4.3V
- Register Timed Access Protection
- Programmable System Clock
- Multi-mode Operation: Normal/Idle/Stop/Sleep
- 16-bit Timers/Counters:
  - ✧ 80C51-like Timer 0 & 1
  - ✧ 8052-like Timer 2 with Compare/Capture Unit (CCU)
- Six 12-bit PWM: PWM0/1/2/3/4/5
  - ✧ PWM0/3 share cycle and control register
  - ✧ PWM1/4 share cycle and control register
  - ✧ PWM2/5 share cycle and control register
  - ✧ Four output mode: standard, center-aligned, register matched set high and matched toggled
- Three channel deathtime wave generate
  - ✧ Rising, falling edge deathtime control
  - ✧ Multiple signal source selection
- BEEPER: 1/2/4 KHz
- Watchdog Timer with Additional Configurable Prescaler: WDT
- UART0/UART1/SPI/I2C Interface
- Analog Digital Converter: ADC
  - ✧ 11-bit resolution
  - ✧ Up to 8 multiplexed channels
  - ✧ support external input VREF
- Analog Comparator: ACMP
- Support In-Circuit Programming: ICP
- Support In-Circuit Debugging: ICD
- ESD: >2KV (HBM)
- EFT: >4KV
- Package Types: SOP16, TSSOP20/24, SSOP24

Memory

- 16K bytes Program Flash
- 256 bytes Data EEPROM（byte/page operation, 1page=64bytes)
- 256 bytes internal scratch-pad RAM
- 1K bytes internal XRAM
- Memory Programming Permission Control
- Flash Cycling: 100K@25℃
- EEPROM Cycling: 500K@25℃
- Data retention: 40 years@25℃

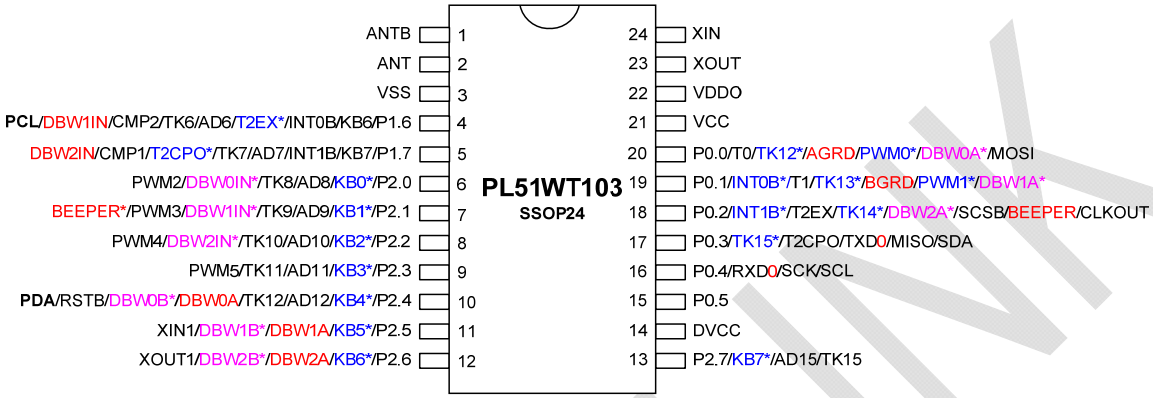
3 Quick Reference Data

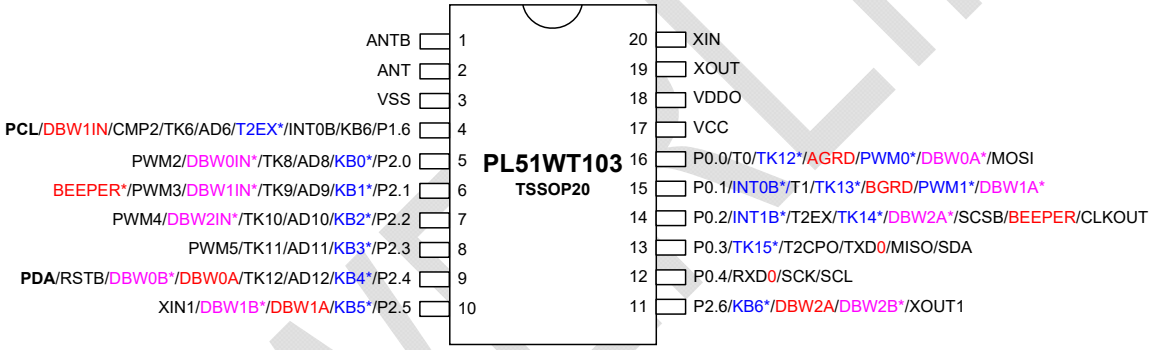
Parameter	Value	Units
Min Supply Voltage	2.4	V
Max Output Power	5.5	dBm
Data Rate	1	Mbps

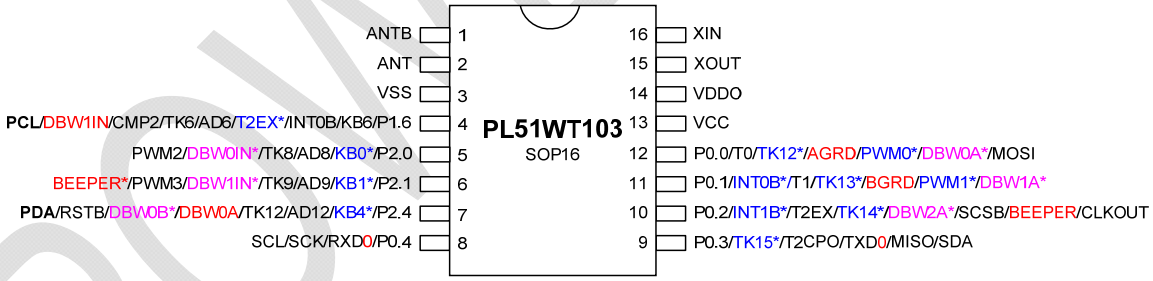
Parameter	Value	Units
Current Consumption (0dBm) @TX Mode	16	mA
Current Consumption @RX Mode	17	mA
Operating Temperature Range	-25 to +105	℃
RX Sensitivity	-88	dBm
RF Crystal Oscillator	12	MHz
CPU core Internal RC OSC Frequency	4/8/12	MHz
CPU core Internal 12MHz RC OSC Precision	±2	%
Current Consumption @ Sleep Mode	3	uA

4 Pin Configurations

4.1 Pin Diagrams







Note：

1) *The outside pin function has the highest priority, and the inner pin function has the lowest priority. It means that if the higher priority function is enabled, the lower priority function can't be used even when the lower priority function is also enabled.*

2) *The pin name colored blue with * denoted the shift ports, the pin function available only when the relative shift control bit in SFR "PSFT0~1" is set.*

3) *Specially： this chip register AUXCON.s003_sopt cannot be set to 1.*

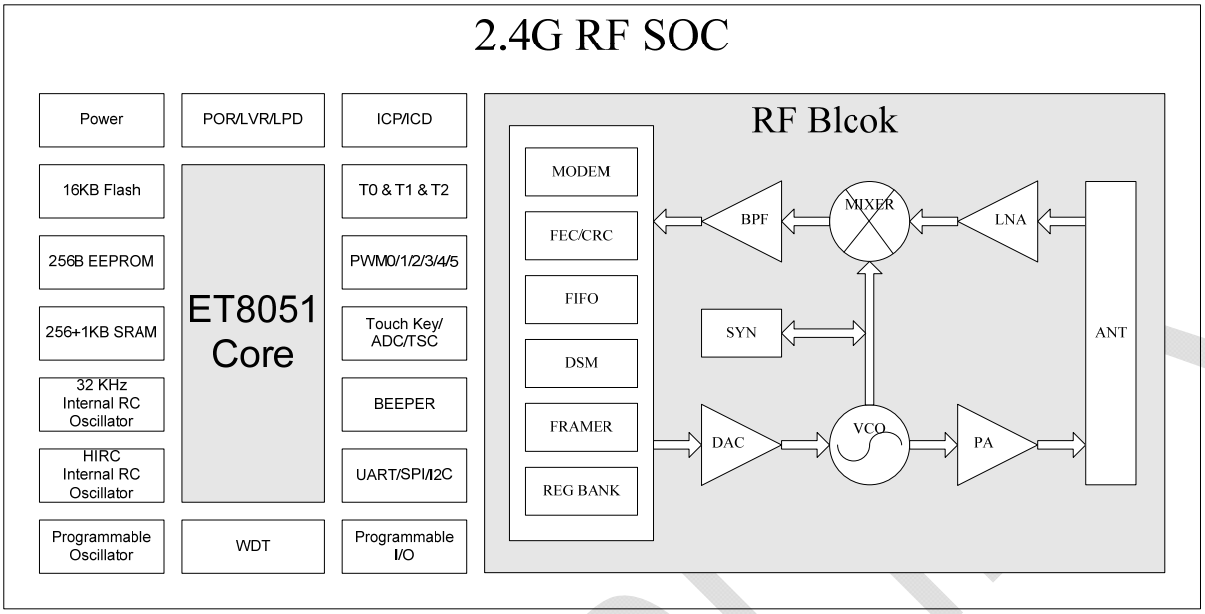
4) *For unused or not led out pins, recommended to configure input pull-up or output fixed lever.*

4.2 Pin Description

Classify	Symbol	Type	Descriptions
Power	VCC	Power	Power Supply (2.4~3.6V)
	VSS	Power	Ground (0V)
	DVCC	Power	Power Supply (2.4~3.6V)
	DVSS	Power	Ground (0V)
	VDDO	Power	1.8V power output, connect to capacitor
RF Block	ANTB	RF	Antenna Interface
	ANT	RF	Antenna Interface
	XIN	Analog Input	12MHz Crystal Oscillator Input of RF
	XOUT	Analog Output	12MHz Crystal Oscillator Output of RF
RF Block Interface	P1.0	Digital Input	Interface of RF block SPI.SDO output
	P1.1	Digital Output	Interface of RF block SPI.SDI input
	P1.2	Digital Output	Interface of RF block SPI.SCK input
	P1.3	Digital Output	Interface of RF block SPI.SCSB input
	P1.4	Digital Input	Interface of RF block FIFO Status Indicator Bit output
	P1.5	Digital Output	Interface of RF block RSTB input
Ext Reset	RSTB	Digital Input	Reset Pin of CPU core, Active Low
Clock	XIN1	Analog Input	Crystal Oscillator Input of CPU core
	XOUT1	Analog Output	Crystal Oscillator Output of CPU core
	CLKOUT	Digital Output	Internal Clock Output of CPU core
UART	RXD0	Digital Input	RXD0 of Serial Port
	TXD1	Digital Output	TXD0 of Serial Port
SPI	SCSB	Digital Input	Enable Input for SPI Interface, active Low
	SCK	Digital I/O	Clock for SPI Interface
	MISO	Digital I/O	Master Data Input or Slave Data Output for SPI Interface
	MOSI	Digital I/O	Master Data Output or Slave Data Input for SPI Interface
I2C	SCL	Digital I/O	Clock for I2C Interface
	SDA	Digital I/O	Data I/O for I2C Interface
Timer0	T0	Digital Input	Timer 0 Input
Timer1	T1	Digital Input	Timer 1 Input

Classify	Symbol	Type	Descriptions
Timer2	T2 EX	Digital Input	Timer 2 external reload or gate Input
	T2CPO	Digital Output	T2 compare or PWM output
Ext Interrupt	INT0B	Digital Input	External Interrupt 0
	INT1B	Digital Input	External Interrupt 1
PWM	PWM0	Digital Output	PWM 0 Output
	PWM1	Digital Output	PWM 1 Output
	PWM2	Digital Output	PWM 2 Output
	PWM3	Digital Output	PWM 3 Output
	PWM4	Digital Output	PWM 4 Output
	PWM5	Digital Output	PWM 5 Output
ACMP	CMP2	Analog Input	Comparator channel 2 Input
ADC	AD6~12/ TK15	Analog Input	8 channel AD Input
Touch Key	TK6~12/ TK15	Analog Input	8 channel Touch Key Inputs
Key Board	KB0~7	Analog Input	8 channels Keyboard Inputs
PORT0	P0.0~P0.5	Digital I/O	General purpose I/O Port 0
PORT1	P1.7	Digital I/O	General purpose I/O Port 1
PORT2	P2.0~P2.7	Digital I/O	General purpose I/O Port 2
ICP	PCL	Digital Input	Clock Input for ICP/ICD Mode
	PDA	Digital I/O	Data I/O for ICP/ICD Mode
DBW	DBW0A	Digital Output	Death Wave Generation DBW0A Output
	DBW1A	Digital Output	Death Wave Generation DBW1A Output
	DBW2A	Digital Output	Death Wave Generation DBW2A Output
	DBW0B	Digital Output	Death Wave Generation DBW0B Output
	DBW1B	Digital Output	Death Wave Generation DBW1B Output
	DBW2B	Digital Output	Death Wave Generation DBW2B Output
	DBW0IN	Digital Input	Death Wave Generation DBW0 Iutput
	DBW1IN	Digital Input	Death Wave Generation DBW1 Iutput
	DBW2IN	Digital Input	Death Wave Generation DBW2 Iutput
BEEPER	BEEPER	Digital Output	BEEPER Output

5 Block Diagram



6 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage and affect device reliability if exceeded.

Parameter	Symbol	Value	Units
Supply Voltage of VDD	VDD	-0.3 to +3.6	V
Supply Voltage of VCC	VCC	-0.3 to +3.6	V
Supply Voltage of VDDO	VDDO	-0.3 to +2.5	V
Input Voltage	V_{IN}	-0.3 to (VDD+0.3)	V
Operating Temperature	T_{OP}	-25 to +105	℃
Storage Temperature	T_{ST}	-55 to +150	℃
Maximum Current into VDD	/	100	mA
Maximum Current out of VSS	/	100	mA
Maximum Current suck by a I/O pin	/	10	mA
Maximum Current sourced by a I/O pin	/	10	mA
Maximum Current suck by total I/O pins	/	100	mA
Maximum Current sourced by total I/O pins	/	100	mA

Note: *These are stress ratings only. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.*

7 Electrical Characteristics

7.1 RF Electrical Characteristics

(Conditions：VCC=+3V，VSS=0V，TA=－40℃ to +105℃)

Symbol	Parameter (Condition)	Notes	Min.	Typ.	Max.	Units
	Operating Conditions					
VCC	Supply voltage of VCC		2.4	3.3	3.6	V
T_{OP}	Operating Temperature		-25		105	℃
	General RF Conditions					
f_{OP}	Operating frequency		2402		2480	MHz
f_{XTAL}	Crystal Frequency			12		MHz
△ f_{1M}	Frequency Deviation @1Mbps			280		KHz
R_{GFSK}	Data Rate			1		Mbps
$F_{CHANNEL}$	Channel Spacing			1		MHz
	Transmitter Operation					
P_{RF}	Maximum Output Power			0	5.5	dBm
P_{RFC}	RF Power Control Range		18	20	22	dB
P_{RF1}	1st Adj. Channel TX Power				-20	dBm
P_{RF2}	2nd Adj. Channel TX Power				-50	dBm
I_{VCC_H}	Power Consumption @High Gain			16		mA
I_{VCC_L}	Power Consumption @Low Gain			12		mA
	Receiver Operation					
I_{VCC}	Power Consumption			17		mA
RX_{SENS}	RX Sensitivity @0.1%BER			-88		dBm

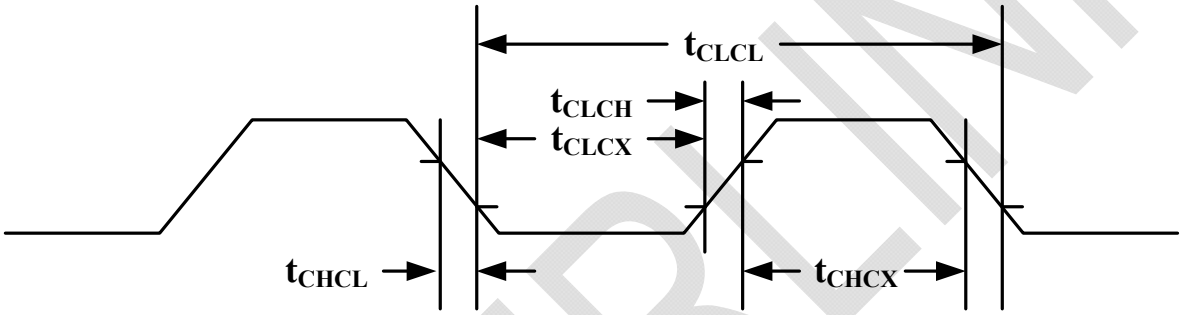
7.2 DC Electrical Characteristics

(VDD = 2.4V~3.6V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Operating Voltage	VDD	2.4	3.3	3.6	V	CPU core Freq: ~12MHz
Operation Current	I_{OP}		2		mA	No load, VDD=3.3V@8MHz
IDLE Current	I_{IDLE}		1		mA	No load, VDD=3.3V@8MHz, IDLE
STOP Current	I_{STOP}		5		uA	No load, VDD=3.3V, STOP
SLEEP Current	I_{SLEEP}		3		uA	No load, VDD=3.3V, SLEEP
Input High Voltage	V_{IH}	0.7*VDD		VDD+0.2	V	
Input Low Voltage	V_{IL}	-0.5		0.3*VDD	V	

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Output High Voltage	V_{OH}	2.6			V	VDD=3.3V, I_{OH}=-10mA
Output Low Voltage	V_{OL}			0.7	V	VDD=3.3V, I_{OL}=+10mA
Port Pull up Resistor	R_{PU}		100		KΩ	
POR slope rate	S_{POR}	0.025		4.5	V/ms	
POR threshold voltage of rising	V_{PORH}		1.6		V	
POR threshold voltage of falling	V_{PORL}		1.2		V	

7.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

7.3.1 External Clock Characteristics

(VDD = 2.4V~3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency			12		MHz	
Clock High Time	t_{CHCX}	30			ns	
Clock Low Time	t_{CLCX}	30			ns	
Clock Rise Time	t_{CLCH}			10	ns	
Clock Fall Time	t_{CHCL}			10	ns	

7.3.2 Internal RC OSC Characteristics

(VDD = 2.4V~3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency			8/12		MHz	
Clock Frequency			±2		%	T_A = 25°C

7.3.3Crystal Oscillator/Ceramic Resonator Characteristics

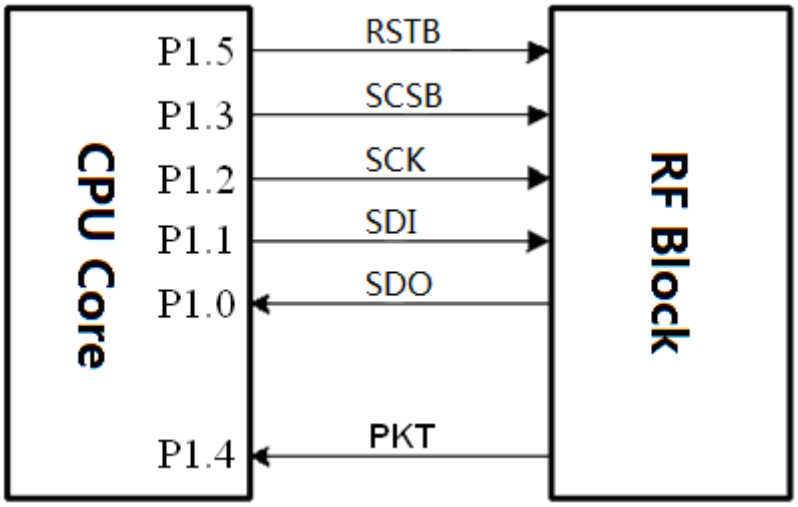
(VDD = 2.4V~3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Specification				Test Conditions
		Min.	Typ.	Max.	Units	
Clock Frequency		400K		12M	Hz	

8 Internal RF Interface

8.1 SPI Data and Control

The RF block provides a simple CPU Core SPI interface for application. The RF block SPI supports slave mode only.

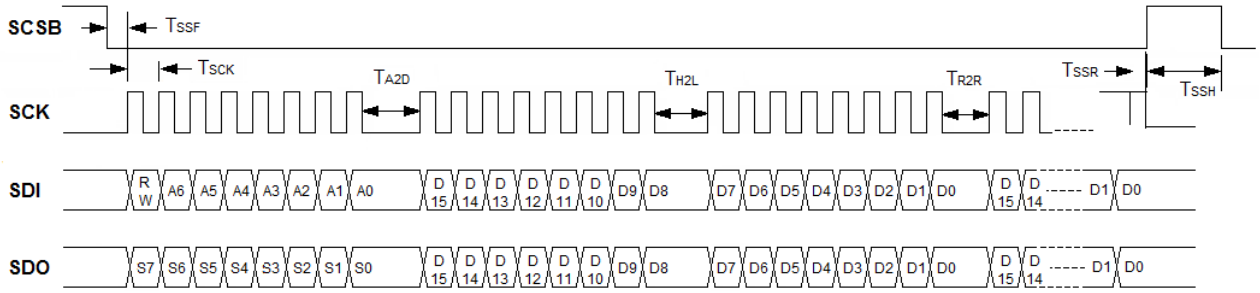


The data and control interface gives access to all the features in the chip. The data and control interface consists of the following six digital signals:

Pin	Description
RSTB	Reset Input, active low
SCSB	SPI Slave Select Input Wakeup from SLEEP state
SCK	SPI Clock Input
SDI	SPI Data Input
SDO	SPI Data Output
PKT	Packet TX/RX Flag

Note: can set rfspi_sft(code5.7) as 1, using hardware MCU-SPI connect RF.

8.2 SPI Command Format



***Note**: The device SPI bus setup data when the rising edge of the master SCK, and sample data at the falling edge of the master SCK.*

Name	Min.	Typ.	Max.	Description
T_{SSH}	250ns			Interval between two SPI accesses
T_{SSF}, T_{SSR}	41.5ns			Relationship between SCSB and SCK
T_{A2D}	*1			Interval time between address and data
T_{H2L}	*1			Interval time between high byte and low byte data
T_{R2R}	*1			Interval time between two register data
T_{SCK}	83ns			SCK period

***Note**: *1--When reading FIFO data, at least 450ns wait time is required. Otherwise, $T3_{min}$ = 41.5ns.*

9 Memory

The Memory contains 16K bytes program code Flash, 256 bytes data code EEPROM.

- 16K bytes program Flash
- 256 bytes data EEPROM

9.1 Memory Encryption

The program code area is encrypted with a proprietary high security level in this device.

9.2 Register Definition

9.2.1EEPROM Control Register – EECON

Table 9-1 EECON Register (97h)

Bit	Symbol	Description	Type	Reset
eecon.7	LOCK	**EEPROM program inhibit** 0 – EEPROM program is enabled 1 – EEPROM program is inhibited	R/W	0
eecon.6	-	-	-	0
eecon.5	-	-	-	0
eecon.4	-	-	-	0
eecon.3	EPGM	**EEPROM program interrupt enable** When epgm=0 EEPROM program interrupt is disabled. When epgm=1 and ea=1 EEPROM program interrupt is enabled.	R/W	0
eecon.2	PGMF	**EEPROM program interrupt flag** 1 – EEPROM program is finished It can only be set by hardware and can be cleared by software or interrupt. When set PGM to 1, it will be cleared automatically.	R/W	0
eecon.1	CPF	**EEPROM program cross page flag** 1 – EEPROM program page is changed (cross page) If CPF=1, PGM can not be set to 1 until CPF is cleared by software. CPF can only be set to 1 by hardware, it can not be set to 1 by software.	R/W	0

Bit	Symbol	Description	Type	Reset
		After cross page error occurred, more than 3 NOP must be followed close behind the CPF cleared instruction to avoid the reset operation of EEPROM.		
eecon.0	PGM	**EEPROM program enable** 1 – start EEPROM program After write data to EEPROM buffer, set it to start EEPROM program. If EEPROM buffer is not written, software can not set it. When program is finished, it is cleared by hardware automatically. It can not be cleared by software.	R/TW	0

10 ICP (In-Circuit Programming)

The contexts of flash in the device are empty by default. User must program the flash by external Writer device or by ICP (In-Circuit Programming) tool.

In the ICP tool, the user must take note of ICP's programming pins used in system board. In some application circuits, it is highly recommended customer power off then power on after ICP programming has completed on the system board.

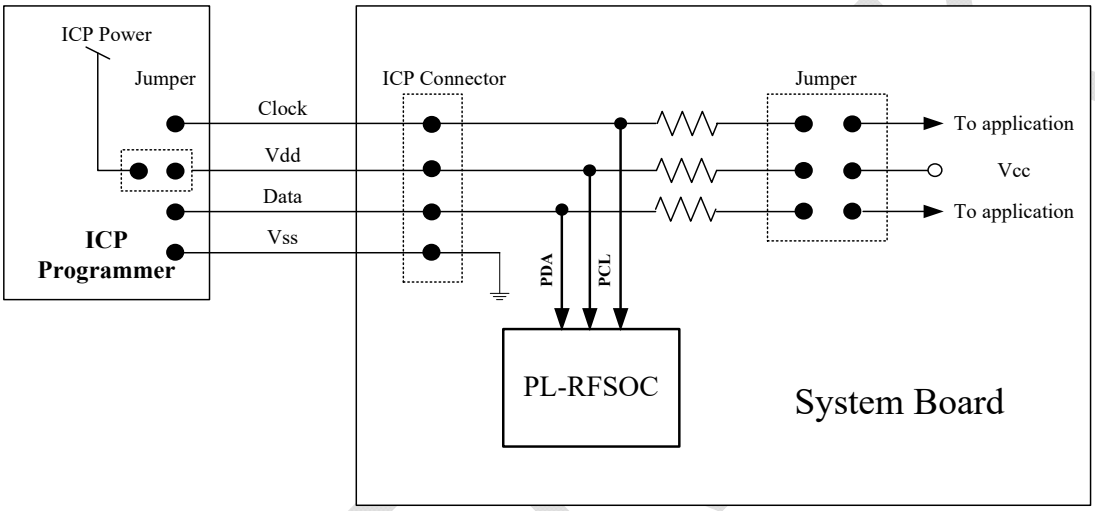


Figure 10-1 ICP Application Circuit

Note:

1. *Circuitry separation is optionally needed between ICP and application during ICP operation.*
2. *Resistor is optional by application*
3. *When using ICP to upgrade code, the clock PCL and data PDA must be taken within design system board.*
4. *After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.*

The device supports programming of Flash (4K bytes AP Flash), and data EEPROM (128 bytes). User has the option to program the AP Flash and data EEPROM either individually or both.

11 ICD (In-Circuit Debugging)

The ICD implements functions which allow to stop/run/step the CPU.

- 2-pin access to your on-chip
- Efficient use of the 2-pin interface for both test and debug

ICD debug pin PCL and PDA can be controlled by enabling Option bit CODE1.7(ICDPEN); When CODE1.7 is 0, the ICD debug pin disabled; When CODE1.7 is 1, enable ICD debug pin, PCL and PDA are dedicated to ICD debug.

12 Config Options

The follow config options user can configure in programming software interface.

Config Option	Config Option
Program area Flash lock 0 – Lock 1 – Unlock	**Data area EEPROM lock** 0 – Lock 1 – Unlock
Flash ROM area enable 0 – Does not cure into ROM 1 – Cured into ROM	**Flash ROM area size select** 0 – High 4K as ROM area 1 – High 8K as ROM area
RSTB reset pin enable 0 – Disable 1 – Enable	**ICD debug pin enable** 0 – Disable 1 – Enable
Oscillator type select 00 – Internal high frequency RC (4~12MHz) 01 – Internal low frequency RC (32KHz) 10 – Crystal and ceramic oscillator XTAL 11 – External clock input ECLK	**Internal high frequency RC frequency select** 00 – Internal RC 4MHz 01 – Internal RC 8MHz 10 – Internal RC 12MHz 11 – RSV
XTAL crystal internal res/cap config 0 – Nonuse 15pf internal cap. and feedback res. 1 – Use 15pf internal cap. And feedback res.	**XTAL crystal drive gear adaptation** 000 – 200KHz 001 – 400KHz 010 – 2MHz 011 – 4MHz 100 – 8MHz 101 – 12MHz 110 – RSV 111 – RSV
External clock ECLK config code 00 – LECK low power mode(0MHz~0.5MHz) 01 – MECK medium power mode(0.5MHz~4MHz) 10 – HECK high power mode(4MHz~12MHz) 11 – HECK high power mode(4MHz~12MHz)	
Warm-start time config 00 – The longest ……	**Timeout config** 00 – (16ms+4*4ms retry)*2----------64ms 01 – (16ms+4*4ms retry)+16ms-------48ms

Config Option	Config Option
11 – The shortest *Note: different oscillators Warmup gears different*	10 – (16ms+4*4ms retry)+8ms---------40ms 11 – (16ms+4*4ms retry)+0.125ms----32ms
WDT enable 0x – Disable 10 – Enable, control by WDTEN 11 – Enable, control byWDTEN, disable in stop mode	**WDT enable power-on default config** 0 – Default disable WDT 1 – Default enable WDT(WDT is enabled)
Low voltage reset LVR enable 00 – disable 01 – RSV 10 – enable(in SLEEP mode need turn on) 11 – RSV	**Low power detect LPD enable** 0 – disable 1 – enable
Low voltage reset LVR threshold voltage select 000 – 1.2v 001 – 1.5v 010 – 1.8v 011 – 2.1v 100 – 2.4v 101 – 2.7v 110 – 3.7v 111 – 4.3v	**Low power detect LPD threshold voltage select** 000 – 1.2v 001 – 1.5v 010 – 1.8v 011 – 2.1v 100 – 2.4v 101 – 2.7v 110 – 3.7v 111 – 4.3v
External interrupt trigger supplementary mode release mode select 0 – Released by IFx 1 – Released by intxack	
External interrupt 0 triggers the supplement mode select 00 – Default mode, controlled by it0 & it0_inv 01 – Posedge trigger(internal low level trigger) 10 – Negedge trigger(internal low level trigger) 11 – Dual edge trigger(internal low level trigger)	**External interrupt 1 triggers the supplement mode select** 00 – Default mode, controlled by it1 & it1_inv 01 – Posedge trigger(internal low level trigger) 10 – Negedge trigger(internal low level trigger) 11 – Dual edge trigger(internal low level trigger)

13 CPU Core Information

The detail description of CPU core is in user manual, please contact with POWERLINK.

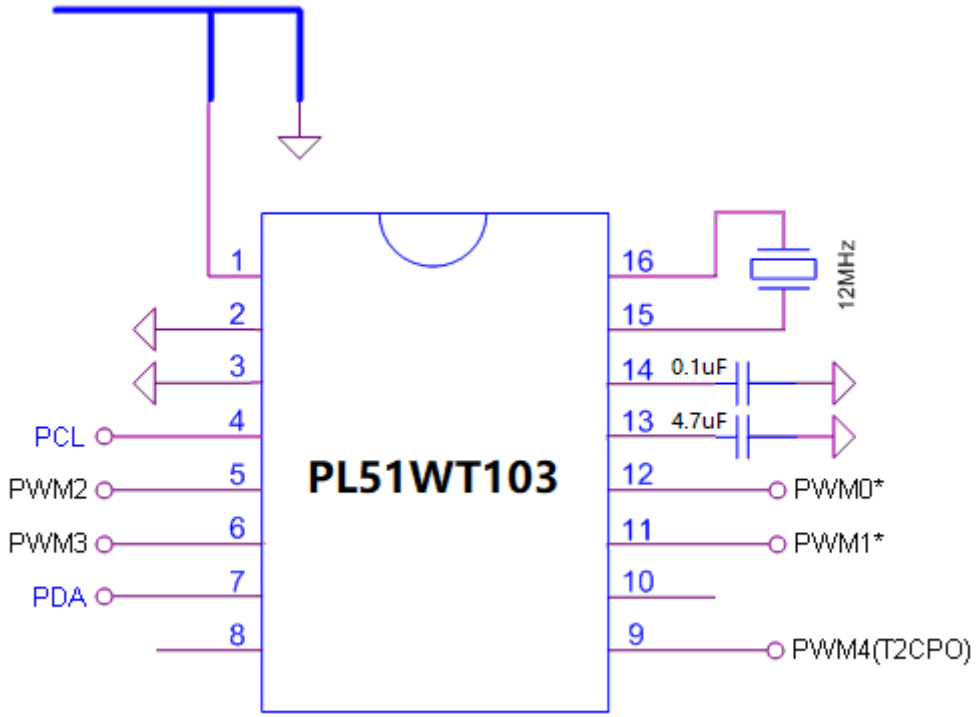
14 RF Block Control Register Information

The latest recommended control registers value is in user manual, please contact with

POWERLINK.

15 Typical Application

15.1 Smart Lighting: RGB+CW/WW

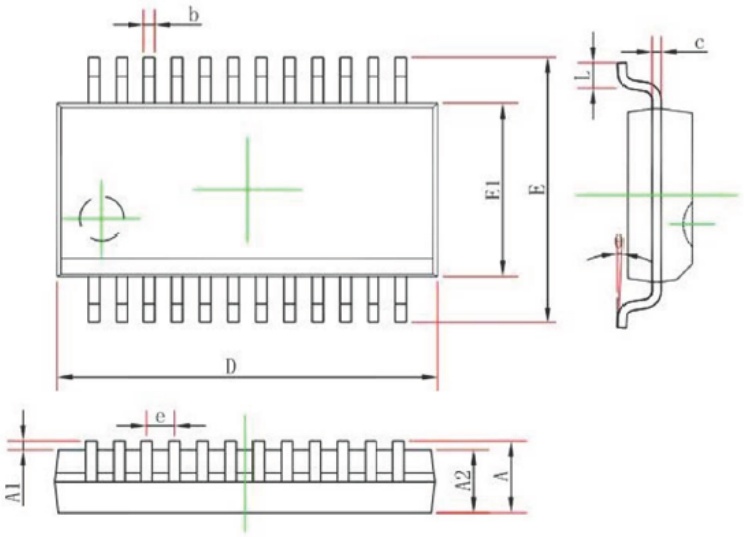


Note: PWM of SOP16 are 4(12-bit)+1(8-bit); TSSOP20/SSOP24 support PWM for 6(12-bit)+1(8-bit), can achieve such as 'RGB+CW/WW+ layered light' and other better function and effect.

16 Package Dimensions

16.1 SSOP24 Package

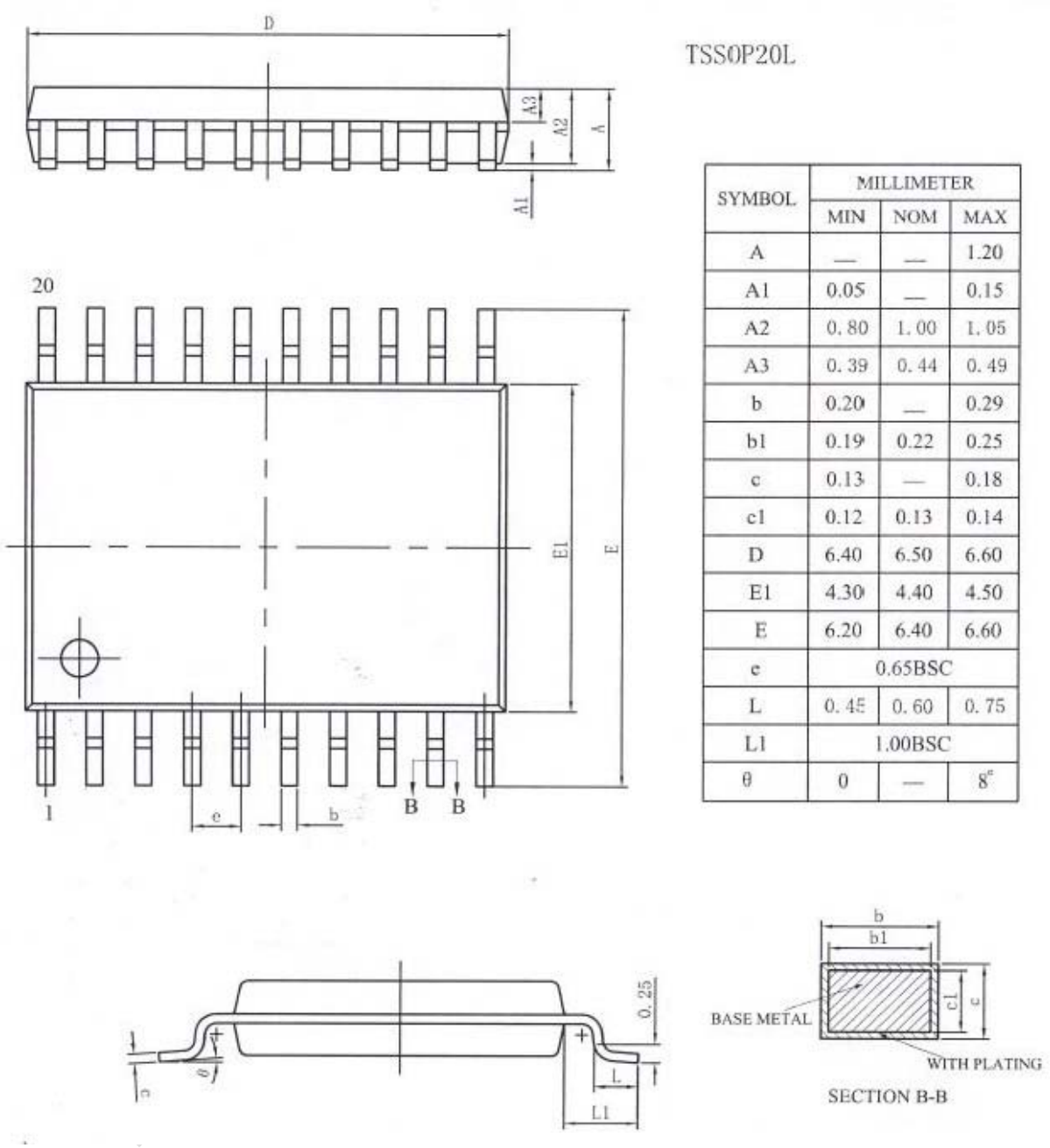
SSOP24 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters	
	Min	**Max**
A	——	1.750
A1	0.050	0.080
A2	1.400	1.500
b	0.203	0.305
c	0.102	0.254
D	8.550	8.650
E1	3.800	4.000
E	5.800	6.200
e	0.635 (BSC)	
L	0.400	1.270
θ	0°	8°

16.2 TSSOP20 Package

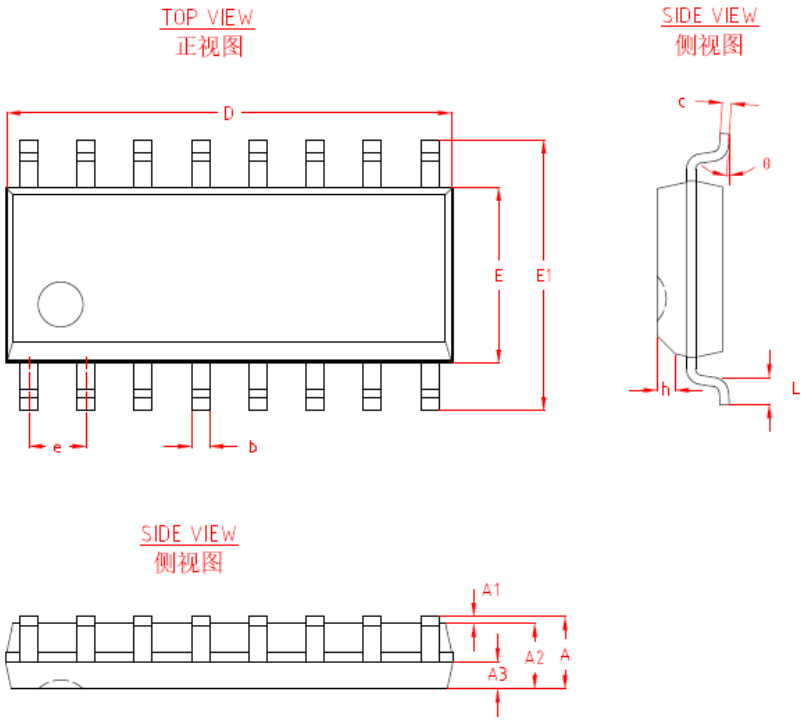
TSSOP20 PACKAGE OUTLINE DIMENSIONS



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

16.3 SOP16 Package

SOP16 PACKAGE OUTLINE DIMENSIONS



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	–	0.50
c	0.19	–	0.25
D	9.80	10.00	10.20
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	–	0.50
L	0.40	–	0.80
θ	0°	–	8°

17 Ordering Information

Part Number	Packaging
PL51WT103S16	SOP16, Tube
PL51WT103S16R	SOP16, Tape&Reel
PL51WT103T20	TSSOP20, Tube
PL51WT103B24	SSOP24, Tube
……	……

18 Document Revision History

Rev.	Date	Comments
0.1	2021/07/28	Initial Version
0.2	2021/08/06	Optimize Pin Definition
0.3	2021/09/06	Optimize SSOP24 Pin Definition
0.4	2021/09/29	Add Register DACCON.s003_sopt Application Notice
0.5	2021/11/04	Updated Operation Parameter
0.6	2022/07/22	Deleted DAC/OPA's Pins
0.7	2023/02/06	Updated PL51T103's pin definition, deleted TKADC-5&13&14

19 Important Notice

POWERLINK reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.